1. A universally accessible fully programmable memory built-in self-test (MBIST) system comprising:

an MBIST controller including:

an address generator configured to generate addresses for a memory under test;

a sequencer circuit configured to deliver test data to selected addresses of said memory under test and reading out that test data;

a comparator circuit configured to compare said test data read out of said memory under test to said test data delivered to said memory under test to identify a memory failure, and

an externally accessible user programmable pattern register for providing a pattern of test data to said memory under test; and

an external pattern programming device configured to supply a said pattern of test data to said user programmable pattern register.

2. The system of claim 1 in which said external programming device includes a computer configured to generate a user defined pattern of test data.

3. The system of claim 1 in which said external programming device includes programmable hardware configured to generate a user defined pattern of test data.

4. The system of claim 1 in which said user programmable pattern register includes FLASH memory.

5. The system of claim 1 further including a switch configured to select a computer or programmable hardware to generate a user defined pattern of data.

6. The system of claim 1 in which said user programmable pattern register serially receives said test data from said external pattern programming device.

7. The system of claim 1 in which said user programmable pattern register receives said test data from said external pattern programming device in a parallel configuration.

8. The system of claim 1 in which said user programmable pattern register includes from 1 to N bits.

9. The system of claim 1 in which said user programmable pattern register is located within said MBIST controller.

10. The system of claim 1 in which said user programmable pattern register is located external to said MBIST controller.

11. The system of claim 1 in which said pattern of test data is chosen from the

group consisting of: a checkerboard pattern, a diagonal pattern, an all 0's pattern, an all 1's pattern, a walking 1's pattern, and a walking 0's pattern, and/or any combination thereof.

12. The system of claim 1 in which said pattern of test data is any defined binary data pattern limited only by the size of said user programmable data register.

13. The system of claim 1 in which said pattern of test data includes any user defined pattern of 1's and 0's.

14. The system of claim 1 further including a multiplexor where a test mode signal selects said addresses generated from said address generator or system addresses based on a predetermined state of said test mode signal.

15. The system of claim 1 further including a multiplexor where a test mode signal selects said pattern of test data or system data based on a predetermined state of said test mode signal.

16. A universally accessible fully programmable memory built-in self-test (MBIST) system, the system comprising:

an MBIST controller including:

an address generator configured to generate addresses for a memory under test;

a sequencer circuit configured to deliver test data to selected addresses of said memory under test and reading out that test data, and

a comparator circuit configured to compare said test data read out of said memory under test to said test data delivered to said memory under test to identify a memory failure;

an externally accessible user programmable pattern register remote from said MBIST controller for providing a pattern of test data to said memory under test; and

an external pattern programming device configured to supply said pattern of test data for said user programmable data pattern register.

17. A universally accessible fully programmable memory built-in self-test (MBIST) method, the method comprising:

generating addresses for a memory under test;

generating for an externally accessible user programmable pattern register a pattern of test data with an external pattern programming device;

programming said user programmable pattern register with said pattern of test data to said memory under test;

delivering test data to selected addresses of said memory under test;

reading out said test data from said selected addresses of said memory under test; and

comparing said test data read out of said memory under test to said test data delivered to said memory under test to identify a memory failure.